Abstract of the Disclosure:

The present invention relates to a novel method for fabricating a storage capacitor designed as a trench or a stacked capacitor and is used in particular in a DRAM memory cell. The method includes steps of forming a lower, metallic capacitor electrode, a storage dielectric and an upper capacitor electrode. The lower, metallic capacitor electrode is formed in a self-aligned manner on a silicon base material in such a way that uncovered silicon regions are first produced at locations at which the lower capacitor electrode will be formed, and then metal silicide is selectively formed on the uncovered silicon regions.

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